研究課題名：MIS 構造素子の放射線照射効果に関する研究

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【研究目的】

宇宙空間は放射線環境であり，宇宙飛翔体に搭載する半導体素子には高い耐放射線性が要求される．特に半導体集積回路の基本構造である MIS 構造の放射線照射効果の把握は，耐放射線性素子開発の上で非常に重要である．これまでに，MIS 構造の絶縁膜として酸化膜・窒化膜の多層構造を有する MNOS (Metal-Nitride-Oxide-Semiconductor) 構造は耐放射線性に優れているという報告があるが，その詳細なメカニズムや各絶縁膜厚の最適化等については，ほとんど議論されていない．そこで我々は，放射線照射による MNOS 絶縁膜中での電荷発生および固定電荷（捕獲電荷）の変化に注目して研究を行ってきた．放射線照射に起因した絶縁膜中電荷の変化は，トランジスタのしきい値電圧変動の主要因であり，電荷捕獲メカニズムの定量的な解明はデバイスの信頼性確保の上で非常に重要となる．本研究の目的は，MNOS 構造を用いた MIS 構造の放射線照射効果の詳細な検討，および耐放射線強化構造としての最適化である．

【研究概要】

酸化膜厚，窒化膜厚の各々異なる MNOS ダイオードを作製し，放射線照射実験 (^{60}Co-γ線, 1[Mrad Si]）を行い，照射前後において電気的特性測定を行った．測定結果より，照射によるミッドギャップ電圧（絶縁膜中電荷密度を反映する電圧）の変化量ΔVmg を評価した結果，ゲートに正の電圧を印加しながら照射を行った場合には，照射により Vng が正方向に変化する膜厚条件が存在することがわかった．これは，MOS 構造では確認できない現象であり，照射により絶縁膜中に電子が捕獲されたことを意味する．一方，照射によるシリコン–酸化膜界面準位密度の増加ΔDit についても評価を行った．ΔDit とΔVmg との関係について評価した結果，ΔDit はΔVmg（絶対値）と共に増加することを確認した．ただし，ΔDit の各絶縁膜厚や照射中のゲート印加電圧に対する明確な依存性は見られなかった．これらの結果は，照射による Vmg の変動が小さな MNOS トランジスタは，照射によるしきい値電圧変動および相互コンダクタンスの減少を抑圧できることを示唆しており，MNOS 構造の耐放射線性素子としての可能性を示すものである．

このような MNOS 構造特有の放射線照射による電荷捕獲現象についてモデル化を行うため，照射前における絶縁膜中の電荷分布について検討を行った．同一の基板上で場所的に膜厚を変化し，電気的特性の膜厚依存性を詳細に評価できる「傾斜エッチング法」を提案し，放射線照射前における MNOS 構造絶縁膜中の固定電荷分布評価を行った．その結果，シリコン-酸化膜界面，および酸化膜–窒化膜界面近傍に正電荷が局在し，また酸化膜–窒化膜界面の電荷量は酸化膜厚増大と共に減少することがわかった．この結果を用いて，照射中の電荷発生・捕獲現象について検討を行った．その結果，シリコン–酸化膜界面近傍の酸化膜中には正孔トラップが，また酸化膜–窒化膜界面近傍の窒化膜中には正孔および電子トラップが局在し，各絶縁膜および半導体空乏層中で照射により発生したキャリアの一部がそれらのトラップに捕獲すると仮定したモデルを用いることにより，ΔVmg の各絶縁膜厚および照射中のゲート印加電圧依存性を精度良く表現できることが明らかとなった．

また，提案したモデルを用いたシミュレーションにより，耐放射線性素子としての最適絶縁膜厚に対する評価を行った．その結果，照射中正のゲート電圧が印加された場合，ΔVmg=0 となるような最適膜厚が存在すること，また絶縁膜の酸化膜換算膜厚が 100nm 以下の場合には，最適膜厚は全吸収線量および印加電圧に大きく依存しないことを示し，MNOS 構造の耐放射線性素子としての可能性を明らかにした．

また，トランジスタ構造を用いた照射実験を目指し，p チャネル型 MNOS 電界効果トランジスタ（p-MNOSFET）の作製プロセスについて評価を行った．その結果，良好な半導体–絶縁膜界面の形成には，不純物（ボロン）拡散処理後の半導体表面洗浄を必要とすること，また，CVD 法により作製したシリコン窒化膜の微細なパターンニングには，窒化膜再表面の不純物層の除去が有効であること　などを見出した．これらの検討結果を基に，ボロン拡散層を有する p-MNOSFET（ゲート長：10ー100μm）を試作し，電気的特性測定を行った結果，デバイスシミュレーションの結果とほぼ同等な良好な特性を得られることを確認した．これらの成果をもとに，膜厚の異なる p-MNOSFET に対し照射実験を行い，照射前後における電気的特性測定を行った．その結果，構築されたモデル計算より得られた最適膜厚を有する MNOSFET を用いた場合，照射によるしきい値電圧の変化が抑圧可能であることが実証され，耐放射線性デバイスとしての MNOS 構造素子の可能性を明らかにした．

【まとめ】

酸化膜・窒化膜の多層構造を有する MIS 構造である MNOS 構造の放射線照射効果について検討を行った．その結果，照射により絶縁膜中に電子が捕獲されるような膜厚条件が存在することを実験により明らかにした．また傾斜エッチング法の開発により，絶縁膜中の電荷は各界面付近に局在していることがわかった．これらの結果をもとに，照射中の電荷発生・捕獲モデルを構築した．その結果，本モデル計算により実験結果を定量的に説明できることがわかった．更にこのモデルを用いたシミュレーションにより耐放射線性素子としての最適絶縁膜を評価した．また，トランジスタ構造素子を試作し，照射実験を行うことにより，耐放射線性デバイスとしての MNOS 構造素子の可能性を明らかにした．

【研究業績等】

・発表論文

(1) 大西一功，松田純夫 (2002) 半導体素子に対する放射線照射効果　ー最近の研究傾向ー，電子情報通信学会誌，Vol.85, No.9, pp.662-669

・著書、解説

(1) 大西一功，藤田実　共著 (2002) 絵ときでわかる　半導体デバイス，オーム社

(2) 高橋芳浩 (2003) 衛星搭載用半導体デバイスに関する研究，テクノニュースちば, Vol.29, pp.10-11

・学会発表

(1) Y. Takahashi and K. Ohnishi (2000) Total Dose Effect of Metal-Nitride-Oxide-Semiconductor Structure, Proc. of the International Workshop on Radiation Effects on Semiconductor Devices for Space Application

(2) K. Ohnishi and Y. Takahashi (2002) Total Dose Effect on MIS structures, The International Workshop on Radiation Effects on Semiconductor Devices for Space Application

(3) 大西一功 (2003) SOI MOS 素子の耐放射線性，第 3 回半導体の放射線照射効果研究会

(4) 芝田利彦，阿部哲男，高橋芳浩，大西一功 (2003) 半導体記憶素子のマッピング方法の検討，第 3 回半導体の放射線照射効果研究会

(5) T. Hirao, T. Shibata, J. S. Laird, S. Onoda, Y. Takahashi, K. Ohnishi, and T. Kamiya (2003) Experimental Study of Single-Event Transient Current in SOI Devices, Radiation and its effects on components and system

(6) 芝田利彦，平尾敏雄，J.S.Laird，小野田忍，神谷富裕，村瀬祐児，高橋芳浩，大西一功 (2004) SOI 素子のシングルイベント耐性に関する研究　ーMOS キャパシタにおけるシングルイベント過渡電流の測定ー，第 4 回半導体の放射線照射効果研究会

(7) 大西一功 (2004) 半導体シングルイベント効果研究の現状，応用物理学関係連合講演会

(8) 高橋芳浩，芝田利彦，村瀬裕児，大西一功，平尾敏雄，神谷富裕 (2004) MOS 構造における重イオン照射誘起電流，応用物理学関係連合講演会

(9) K. Ohnishi (2004) Progress of the Radiation Effects Research on Semiconductor Devices in Japan, The International Workshop on Radiation Effects on Semiconductor Devices for Space Application

(10) T. Hirao, J.S. Laird, S. Onoda, T. Shibata, T. Wakasa, T. Yamakawa, H. Abe, Y. Takahashi, K. Ohnishi, H. Itoh (2004) Charge collected in Si MOS Capacitors and SOI Devices $P^{+}N$ Diodes due to Heavy Ion Radiation, The International Workshop on Radiation Effects on Semiconductor Devices for Space Application

(11) Y. Takahashi, T. Shibata, Y. Murase, K. Ohnishi, T. Hirao, T. Kamiya (2004) Heavy-Ion induced Current in MOS Structure, The International Workshop on Radiation Effects on Semiconductor Devices for Space Application

(12) T. Abe, K. Ohnishi, Y. Takahashi, T. Hirao (2004) Consideration to Reliability of Laser Testing for Evaluating SEU Tolerance, The International Workshop on Radiation Effects on Semiconductor Devices for Space Application

TOTAL DOSE EFFECTS ON MIS STRUCUTRES

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Abstract

Characteristics and role of hydrogen and nitrogen related trap centers effects on radiation induced positive charges and Si-SiO_2 interface states generation were discussed from experimental results of MOS capacitors annealed in H_2, N_2 and ammonia. The charge distributions in insulators of MOS and MNOS were also discussed by using the slanted etching method. Experimental results make clear that the nitrogen related trap center is amphoteric. Most optimum thickness of the oxide and the nitride films of radiation hardened MNOS structure is discussed too.

1. Introduction

Total dose effects on MOS structures have been previously discussed for long time. When a MOS FET and IC are irradiated to ionized radiation, positive charges are induced into the oxide and generate the Si-SiO_2 interface states density increases. The characteristics of devices are changed by this total dose ionizing effects such as the threshold voltage shift, degradation of mutual conductance, increased leakage currents and so on. [1] In this paper, we will summarize our works concerned to total dose effects that have been carrying out in our laboratory since 1985.

The basic mechanisms underlying the oxide charge trapping and interface states generation are explained as follows. Electron-hole pairs are generated in the oxide by ionizing irradiation such as X and gamma rays.[2-3] Some of the pairs recombine there; the rest of them are separated due to the field in the oxide. Electrons are transported to the metal and/or silicon rapidly and holes move slowly through the oxide to the Si-SiO_2 interface because of the large mobility difference between the electron and the hole. [4] Positive charge buildup is produced by trapped holes in the oxide traps close to the Si-SiO_2 interface states and this is discussed in connection with the Eí center.[5] The radiation interface states are believed to be generated from broken bonds of SiH or SiOH at Si-SiO_2 interface by irradiation.[6] Holes transported from the oxide to the interface interact with bonds and break them.[3,7] This interface trap coincides with the Pb center.[5] The relation between hydrogen related trap center and radiation effects on MOS structure is continuing controversial problems.[8-11]

There are many works concerned to radiation hardening gate oxide and gate insulators.[3,7,12-14]
We also have been studied about radiation-hardened oxide and insulator films on the silicon, and estimated the charge distribution through the insulator films.[15]

In this paper we will explain three things as follows; 1) the annealing atmospheres dependency on the radiation effects of the oxide, 2) ammonia annealing effects on the irradiated oxide and trapped charge distribution through the oxide, 3) radiation effects on the MNOS structures and to optimum thickness of insulator films for radiation hardening.

2. The annealing atmosphere dependency on the radiation effects on the oxide

2.1 Experiments

MOS capacitors used in this experiments were fabricated on n-type <100> oriented, 3-6 Ω-cm Si substrates and oxidized in dry oxygen or diluted oxygen with Ar or nitrogen at a temperatures 1000°C or 1100°C, and all the oxidized silicon films were annealed in nitrogen at 950°C. Oxide thickness was grown to 37~100nm and Al gate of 1mm diameter were evaporated and then annealed at 400°C for 10 minutes, 30 minutes and 90minutes in either nitrogen or hydrogen. (This process is called Post Metal-

ized Anneal, PMA.)

^{60}Co-gamma ray irradiation tests were carried out up to the total dose of 500 krad(Si) at the dose rate of 1.0×10^5 rad/h and 1Mrad(Si) at the dose rate of $3\sim4.13\times10^5$ rad/h.

2.2 Experimental Results

Figure 1 shows the MOS C-V characteristics measured at frequencies of 10 kHz, 100 kHz and 1 MHz before and 5 hours after irradiation. This figure shows the frequency difference between before and after irradiation at 1 Mrad(Si), but it does not show at 500 krad(Si). The shift of C-V curves is more negative as the frequency is low and is larger for PMA in nitrogen than in hydrogen.

Figure 2 shows midgap voltages (V_{mg}) and flatband voltages (V_{fb}) estimated from C-V characteristics. V_{mg} and V_{fb} were measured at 5 hours and 70 hours after 1Mrad (Si) and compared with before irradiation, which do not change with measurement frequency. Midgap voltages (V_{mg}) were almost the same at 5 hours and 70 hours after irradiation regardless of measurement frequency. Contrary, flatband voltages depended on measured frequencies. Though it does not shown in Fig. 2, V_{mg} and V_{fb} did not depend on the frequency in the case of 500 krad(Si), the shift of V_{mg} and V_{fb} are around 1V. Figures 3(a) and (b) show the calculated Si-SiO_2 interface states densities (Dit) of MOS capacitors PMA in H_2 and in N_2. Practically, ΔDit and ΔNot decreased with annealing time for PMA in N_2 and increased in H_2 for longer annealing time.[16-17]

We defined the ΔDit and the ΔNot as the difference of the Si-SiO_2 interface states and trapped charge densities between before and after irradiation respectively. Figure 4 shows the corelation between ΔNot versus ΔDit for various process conditions. Figure 5 shows the ratio between ΔDit and ΔNot for the cases PMA in N_2 and in H_2. In Fig. 4, the gradient of the slope of ΔDit against ΔNot shows 0.75, however it changes with oxide thickness for PMA in N_2 and in H_2 as shown in Fig. 5.[18]

2.3 Discussions

The oxide charge of MOS structure is often estimated from the flat bandvoltage shift. However at the flatband condition, Si-SiO_2 interface states above midgap are considered to be an acceptor-like states and states below midgap is donor-like states.[19-23] Therefore, the flatband voltage shifts by the trapped positive charge in the oxide and the negative charged interface states distributed from

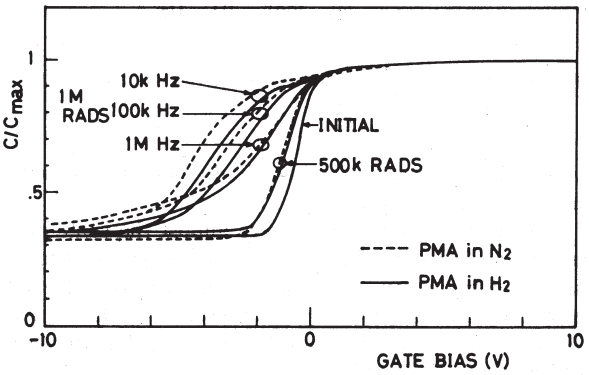


Fig. 1: C-V characteristics of MOS structure before and 5 hours after irradiation.

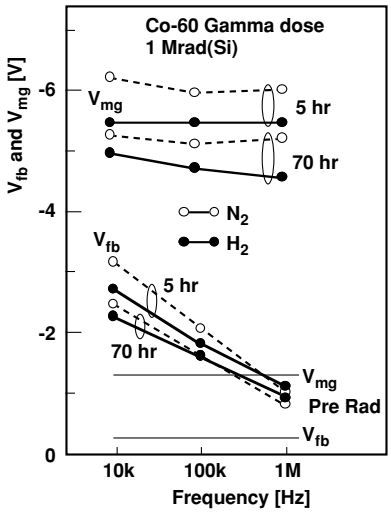
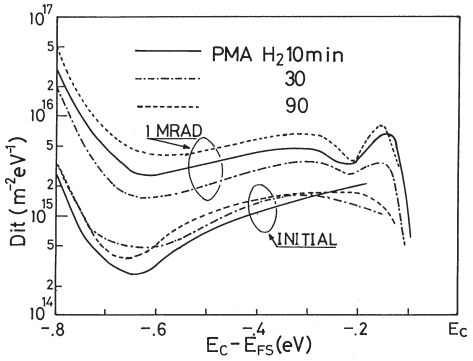


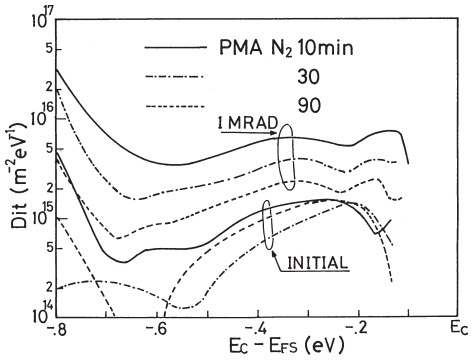
Fig. 2: V_{mg} and V_{fb} of MOS structure before and after irradiation.

midgap to flatband energy levels. If the interface states trap can exchange charges with silicon surface in response to measurement signal, this frequency response makes large the semiconductor capacitance virtually by adding this fast surface states capacitance. C-V curves in Fig. 1 and V_{fb} change in Fig. 2 includes this frequency dependence of fast surface states. When the measurement frequency is high as 1MHz, the interface trap cannot response to the frequency, captured charges are kept trapped in the states and it contribute only V_{fb} shift. The interface trap response to the frequency arround 10kHz to 100kHz has relatively small time constant and coincide with border trap.[24]

The positive charges trapped in the oxide are usually estimated by midgap voltage shift ΔV_{mg} and this seems true from our experiments. We also showed the fact that



(a) PMA in H_2



(b) PMA in N_2

Fig. 3: Si-SiO_2 interface states densities (Dit) of MOS capacitors PMA in H_2 (a) and in N_2 (b).

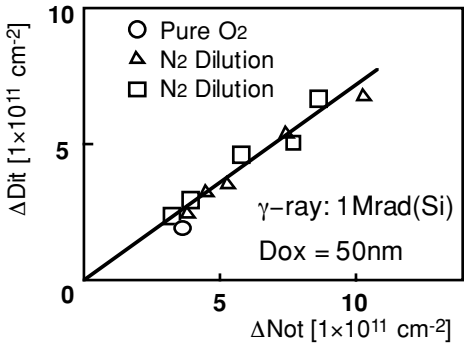


Fig. 4: Relation between ΔDit and ΔNot.

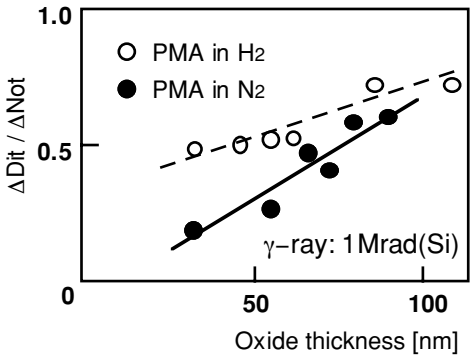


Fig. 5: ΔDit/ΔNot for the cases PMA in N_2 and in H_2.

the increased interface states density after irradiation (ΔDit) is correlated strongly with positive charge buildup due to irradiation as shown in Fig. 4 and it depends on the annealing atmosphere as shown in Fig. 5. ΔNot and ΔDit of MOS capacitor PMA in H_2 was larger than PMA in N_2. From these results, we conclude that the introduced hydrogen during oxidation process break the weak bonding Si-O, and bond with it to make Si-H or Si-OH in the oxide. Hydrogen also bonds with oxygen vacancy in the oxide and making same defects. The hydrogen combines with silicon dangling bond at the Si-SiO_2 interface and making Si-H. These hydrogen related defect bonds can be precursor of radiation introduce positive charge and generate the interface states. When the MOS structure is radiated by ionizing radiation, Si-H and Si-OH can be break easily by irradiation and capture holes (E' center) and generate the Si-SiO_2 interface states (Pb center).

3. Ammonia annealing effects on the irradiated oxide and trapped charge distribution through the oxide

3.1 Experiments

In this experiment, we used the n-type <100> oriented, 0.8-8 Ω-cm Si wafers and oxidized in dry oxygen at a temperatures 1000°C and then annealed in N_2 for 30minutes at same temperature. Ammonia annealing was carried out for 0.5, 1, 3 hours at 950°C and 1000°C, and then anneal in N_2 for 30minutes. Oxide thickness was grown to 20~100nm and Al gate of 1mm diameter were evaporated and then PMA in N_2 at 400°C for 30 minutes. ^{60}Co-gamma ray irradiation tests were carried out up to the total dose of 1Mrad(Si) at the dose rate of 5×10^5 rad/h.

We also tried to estimate the charge distribution through the oxide by using the slanted etching method that we proposed formally, and it can be estimated by measure the midgap voltages of the MOS structures with different thickness of oxide on the same substrate which were prepared by the slanted etching method.[15]

3.2 Experimental results

Figure 6 shows the V_{fb} characteristics of MOS capacitors annealed in ammonia at 950°C and 1000°C, and shows the V_{fb} depends on annealing time and annealing temperature. Figures 7 and 8 show the ΔV_{mg} and ΔDit of ammonia annealed MOS capacitors after irradiation.[25] Figure 9

shows the composition of the oxide annealed in NH_3 at 950 °C analyzed by X-ray Photoelectron Spectroscopy (XPS). Nitrogen density mounted up near the Si-SiO_2 interface and the surface of the oxide.

Figure 10 shows the midgap voltages of the MOS capacitors prepared by slanted etching method. MOS capacitors used in this experiments were oxidized at 1045°C in dry O_2 with standard fabrication process in our laboratory, and the annealed in ammonia for 0,30 60 nd 180 minutes.

The second derivative of V_{mg} to the thickness manifests the density of trapped charge at the point x as following equation.

$$\rho(x) = \frac{d}{dx}(\varepsilon_0 \varepsilon_{ox} E_{ox}) = -\varepsilon_0 \varepsilon_{ox} \frac{d^2 V_{mg}(x)}{dx^2} \quad (1)$$

When charges are distributed in the form of Gaussian, the profile of the charge estimated from Fig. 10 would be shown in Fig. 11. This figure shows that the ammonia annealing causes charge trap centers at around 10 to 20nm near Si-SiO_2 surface and almost coincide with mounted nitride density distribution. From these experiments, it is cleared that the characteristic of nitride related trap center is amphoteric. Figure 12 shows mid-gap voltage distribution after irradiation and Fig. 13 shows the trapped charge distribution.

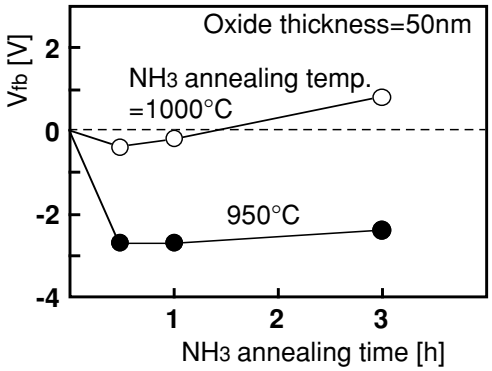


Fig. 6: V_{fb} characteristics of MOS capacitors annealed in ammonia at 950°C and 1000°C.

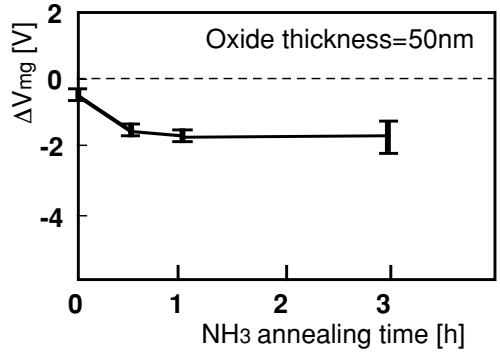


Fig. 7: ΔV_{mg} of ammonia annealed MOS capacitors after irradiation.

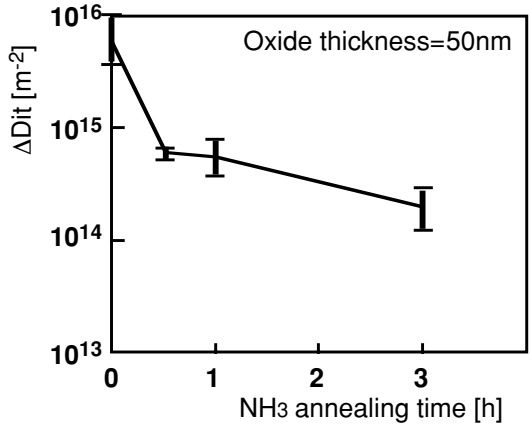


Fig. 8: ΔDit of ammonia annealed MOS capacitors after irradiation.

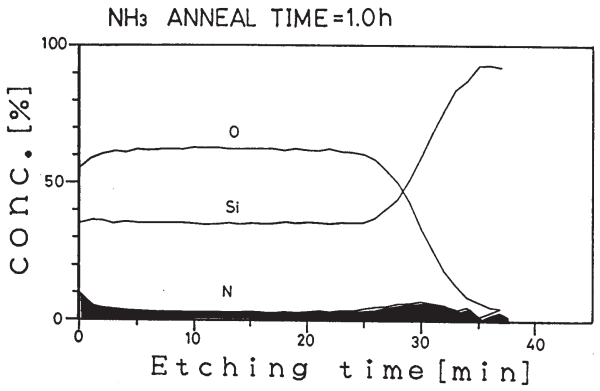


Fig. 9: Composition of the oxide annealed in NH_3 at 950 °C analyzed by XPS.

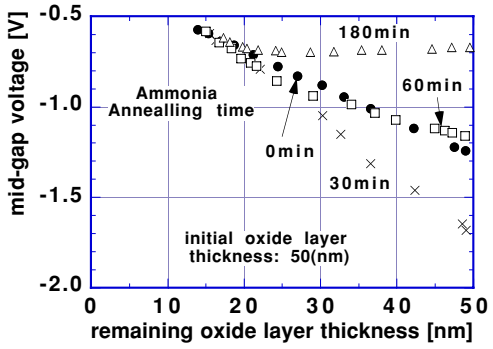


Fig. 10: Midgap voltages of the MOS capacitors prepared by slanted etching method.

3.3 Conclusions

Ammonia anneal after oxidation is effect to reduce the generation of Si-SiO_2 interface states by irradiation. Ammonia annealing does not effective to decrease the charge trap center affects to mid-gap voltage until oxide thickness is 500nm. This trap center distribution is almost same with nitrogen distribution near Si-SiO_2 interface, and the trap is amphoteric.

4. Radiation effects on the MNOS structures and to optimum thickness of insulator films for radiation hardening.

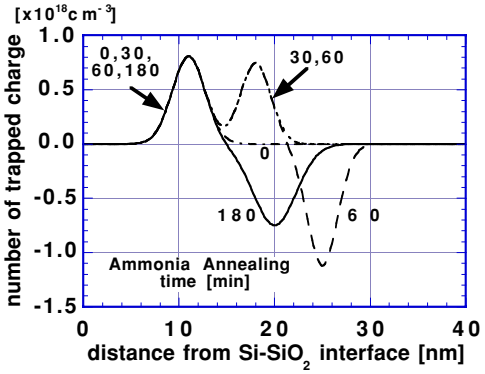


Fig. 11: Estimated charge profile in oxide layer annealed in NH_3 before irradiation.

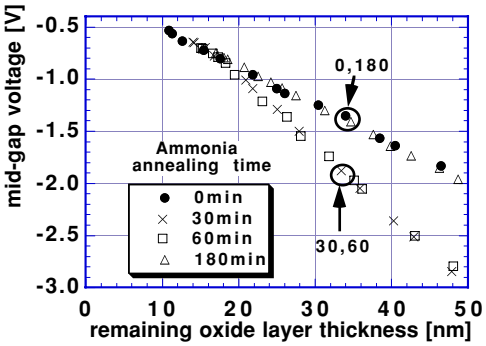


Fig. 12: Midgap voltages distribution of MOS structure after irradiation.

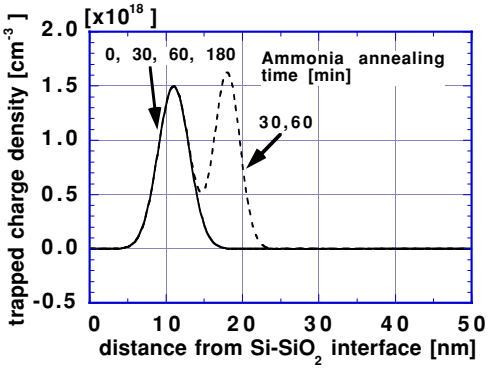


Fig. 13: Estimated charge profile in oxide layer annealed in NH_3 after irradiation.

4.1 Experiment

Figure 14 is the energy band diagram and charge generation and trapping model of MNOS structures by ionized irradiation. MNOS capacitors used in this experiments were fabricated on n-type <100> substrate. Oxide was grown at 1040°C in dry O_2. Nitride layer was deposited on the oxide by LPCVD at 700°C with flow ratio of NH_3 to SiH_2Cl_2 is 3:1. Al electrode formed by vacuum deposition. MNOS capacitors were irradiated to ^{60}Co-gamma ray up to 1Mrad(Si) at dose rate with 5×10^5rad(Si)/h.

4.2 Experimental Results

Figure 15 shows the midgap voltage V_{mg} of MNOS capacitors before and after irradiation. V_{mg} characteristic after irradiation varied the gradient of the slope at the Si_3N_4 and SiO_2 interface. [26] This shows that charges are trapped at SiO_2-Si_3N_4 interface due to irradiation. Figure 16 shows the ΔV_{mg} of MNOS capacitor with oxide thickness is 70 and 120nm for various nitride thickness. The gate voltages during irradiation were +6V and –6V. This figure suggests the negative charges trapping in the insulators when the gate bias is positive. In MOS capacitors, generally positive charges are trapped in the oxide by irradiation. However, nitride related trap center is able to capture the positive and negative charges. From this point of view, we simulate the radiation induced charge trapping using electron and hole trapping model at the Si-SiO_2 interface and SiO_2-Si_3N_4 interface and also calculate the optimum thickness of nitride and oxide films to radiation tolerant. Figure 17 shows the simulated ΔV_{mg} of the MNOS capacitor irradiated at 1Mrad(Si) for the combination of oxide layer thickness and nitride layer thickness when the gate voltage is 5V.

4.3 Conclusions

By using the slant etching method, the charge depth profiles were estimated before and after irradiation. Trapped charges were located mainly at the Si-SiO_2 and SiO_2-Si_3N_4 interfaces, and density at SiO_2- Si_3N_4 was changed by the oxide thickness.

5. Conclusion Remarks

From this work, we infer that the hydrogen in the oxide affects importantly to the radiation induced positive charge and Si-SiO_2 interface states generation due to break

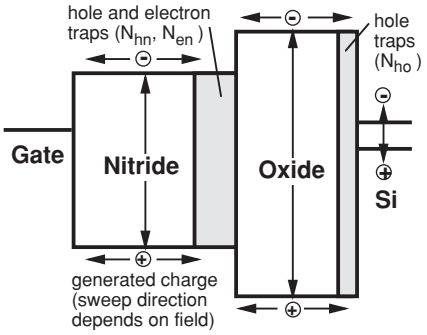


Fig. 14: Charge generation and trapping model of MNOS structure by ionized irradiation.

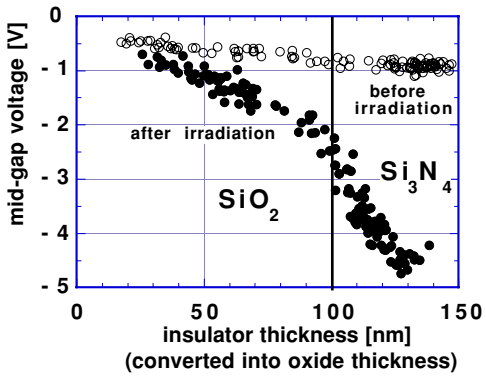


Fig. 15: V_{mg} of MNOS capacitors before and after irradiation.

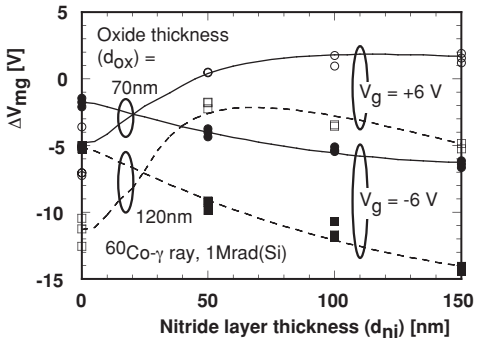


Fig. 16: ΔV_{mg} of MNOS structures due to irradiation.

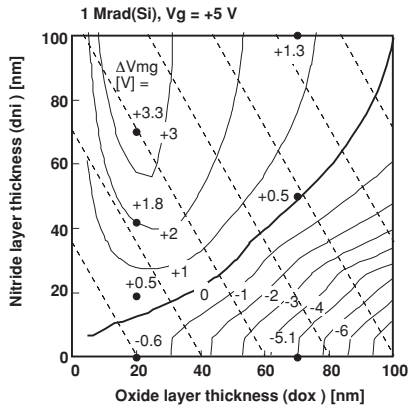


Fig. 17: Simulated ΔV_{mg} of the MNOS structure.

the hydrogen related bonding site. Nitrogen related bonding site has an amphoteric trap, so that this trap captures the positive and the negative charges. This allows to compensate the charges captured in the insulators. MNOS structure is a candidate of the radiation-hardened insulator for IC by using the nitride related trap site. We also proposed the slanted etching method to determine the trapped charge distribution and it can be applied to the complex insulator films such as MNOS structure.

References

(1) T.P.Ma and P.V.Dressendorfer, Ionizing Radiation Effects in MOS Devices and Circuits (John Wiley & Sons, New York, 1989).

(2) P.S.Winokur, J.M.McGarrity and H.E.Boesh,Jr., IEEE Trans. Nucl.Sci. NS-30 (1976) 1580.

(3) F.B.McLean, IEEE Trans.Nucl.Sci. NS-27 (1980) 1651.

(4) R.C.Hughes, Appl. Phys. Lett. 26 (1975) 436.

(5) P.M.Lenahan and P.V.Dressendorfer, J.Appl.Phys. 55 (1984) 3945.

(6) A.G.Revesz, J.Electrochem.Soc.126 (1979) 122.

(7) S.K.Lai, Appl Phys. Lett. 39 (1981) 51.

(8) P.M.Lenahan and J.F.Conelt ,Jr. IEEE Trans.Nucl. Sci. 45 (1998) 2413.

(9) S.T.Pantelides, S.N.Rashkeev, R.Buczko, D.H.Fleetwood and RE.D.Schrimph, IEEE Trans. Nucl. Sci. 47 (2000) 2262.

(10) P.E.Bunson, M.Di.Ventra,S.T.Pantelides, D.M.Fleetwoodand R.D.Scrimph, IEEE Trans.Nucl.Sci. 47 (200) 2289.

(11) S.N.Rashkeev, D.M.Fleetwood, R.D.Schrimph and S.T.Pantelides, IEEE 48 (2001) 2086.

(12) E.H.Nicpllian and J.R.Brews, MOS Physics and Technology (John Wiley & Sons, New York (1982).

(13) R.R.Razouk and B.E.Deal, J.Electrochem. Soc.126 (1979) 1573.

(14) K.K.Hung and Y.C.Cheng, J.Appl.Phys. 59 (1986) 816.

(15) Y.Takahashi, K.Ohnishi, T.Hujimaki and M.Yoshikawa, IEEE Trans. Nucl. Sci. 46 (1999) 1578.

(16) K.Ohnishi and A.Ushirokawa, Transact. IEICE, 70 (1987) 804.

(17) K.Ohnishi and A.Ushirokawa, Japanese J.Appl.Phys. 28 (1989) 877.

(18) K.Ohnishi, Extended Abstract of the 21st Conference on Solid State Devices and Materials Aug. 1989 Tokyo Japan.

(19) T.P.Ma, J.R.Scoggan and R.Leone, Appl.Phys.Lett. 27 (1975) 61.

(20) G.A.Scoggan and T.P.Ma, J.Appl.Phys. 48 (1977) 294.

(21) M.K.Knoll, D.Brauning and W.R.Fahner, IEEE Trans.Nucl. NS-29 (1982) 1471.

(22) C.T.Sah, IEEE Trans.Nucl.Aci. NS-23 (1976) 1563.

(23) K.L.Nagi and C.T.White, J.Appl.Phys. 52 (1981) 320.

(24) D.M.Fleetwood, ì A First-Principles Approach to Total-Dose Hardiness Assurance," 1995 NSREC Short Course, July 17, 1995 Madison Winsconsin.

(25) Y.Hirose, Y.Takahashi, and K.Ohnishi, IEICE SDM-132, July 1990 (in Japanese).

(26) K.Ohnishi, Y.Takahashi, S.Imaki, K.Okada and M.Yoshikawa, The 21st International Symposium for Testing and Failure Analysis Conference Proceedings p.269, Nov. 1995, Santaclara Cal.

TOTAL DOSE EFFECT OF METAL-NITRIDE-OXIDE-SEMICONDUCTOR STRUCTURE

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Abstract

The radiation-induced trapping charge in the insulation layer and generation of interface state of Metal-Nitride-Oxide-Semiconductor (MNOS) structure have been investigated. The irradiation tests were carried out using Co-60 gamma ray source up to 1 Mrad(Si) with the gate voltage of +6 or −6 V. The charge trapping mechanism under irradiation is studied by the radiation-induced mid-gap voltage shift. The simple trap model was proposed to calculate the voltage shift, and it was confirmed that the calculated results can be fitted well to the experimental results. The strong correlation was observed between the mid-gap voltage shift and the generation of interface state. From these results, the optimum oxide and nitride thicknesses for radiation hardened device are evaluated.

1. Introduction

When a MOS structure is irradiated by gamma rays, the positive charge build-up at Si-SiO_2 interface and the interface state creation occur [1]. A Metal-Nitride-Oxide-Si (MNOS) structure which has stacked insulation layers composed silicon nitride and silicon dioxide has been reported to reduce these irradiation effects [2]-[5]. It has been also reported that the flat-band voltage shift due to irradiation depends on both the applied gate voltage during irradiation and the insulation layer thickness.

In this study, the radiation-induced trapping charge in the insulation layer and generation of interface state of MNOS structure have been investigated. The charge trapping during irradiation is discussed by analyzing the radiation-induced mid-gap voltage shift (ΔV_{mg}). The charging in the interface state is neutral at the mid-gap condition. That indicates the ΔV_{mg} is not affected by the interface state generation and is very useful to investigate the radiation-induced charge trapping in the insulation layer. A simple charge trap model is proposed to assess the charge trapping mechanism, and the ΔV_{mg} is calculated using the model. By fitting the calculated results to the experimental results, the charge generation rate and the charge trap densities in the insulators and these capture cross sections are evaluated. The optimum oxide and nitride thicknesses for minimizing ΔV_{mg} are evaluated by the simulation, and the possibility of MNOS structure for radiation hardened device is discussed.

2. Experiments

The MNOS capacitors were fabricated on n-type Si <100> substrates. After conventional cleaning processes, thermal oxidation was performed at 1040˚C in dry O_2 ambient. Following the oxidation, the samples were annealed in N_2 ambient at 1040˚C for 60 min. Nitride layer was deposited on the oxide by LPCVD at 700˚C with the gas flow ratio of NH_3 to SiH_2Cl_2 is 3 : 1. Capacitors were

formed by vacuum deposition of aluminum electrodes (1mm of diameter). The obtained capacitors were irradiated to Co-60 gamma rays up to 1 Mrad(Si) at room temperature. The dose rate was 500 krad(Si)/h. The gate voltage (V_g) of +6 or −6 V was applied during irradiation. High-frequency (1 MHz) C-V characteristics were measured before and after irradiation to evaluate the mid-gap voltage (V_{mg}) and the density of interface state (D_{it}).

3. Experimental Results

Figure 1 shows the ΔV_{mg} of MOS structures as a function of the oxide thickness (d_{ox}). V_{mg} shifts toward negative due to irradiation. The negative shift indicates the radiation-induced holes are trapped in the oxide layer. Figure 2 shows the ΔV_{mg} of MNOS structures in which d_{ox} = 70 and 120 nm as a function of the nitride thickness (d_{ni}). The negative shift is observed regardless of the insulator thickness when V_g = −6 V, and the positive shift is observed when V_g = +6 V. In the case when V_g is positive, ΔV_{mg} changes toward positive with d_{ni}, and is saturated or decreased when d_{ni} becomes thick. It is considered that these phenomena are caused by the radiation induced trapped charges in nitride layer.

Figure 3 shows the radiation-induced increase of the density of interface state (ΔD_{it}) in MOS and MNOS structures as a function of the magnitude of ΔV_{mg}. In this study, D_{it} is determined as average density from mid-gap to fermi energy and is evaluated by the diference of flat-band voltage and V_{mg}. It is found that ΔD_{it} increases with ΔV_{mg}, and the strong correlation can be observed between ΔD_{it} and ΔV_{mg}. However the definite relations with the insulation layer thicknesses and with the gate voltage are not observed.

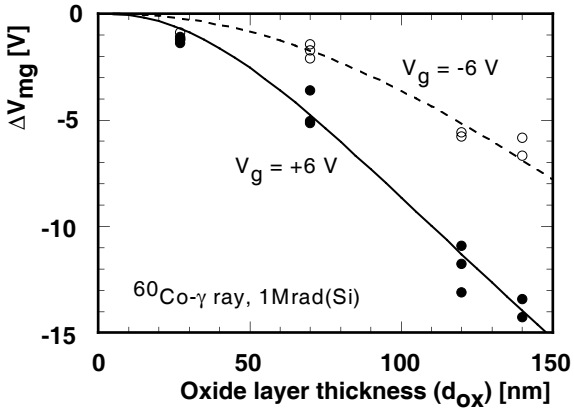

Figure 1: Radiation-induced V_{mg} shift of MOS structures. Points show the experimental results. Lines show the calculated results.

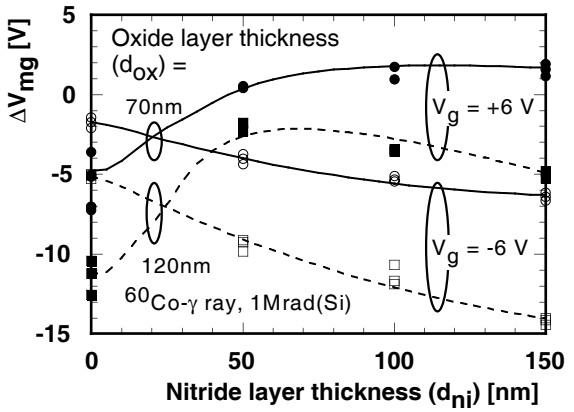

Figure 2: Radiation-induced V_{mg} shift of MNOS structures in which the oxide thicknesses are 70 and 120 nm. Points show the experimental results. Lines show the calculated results.

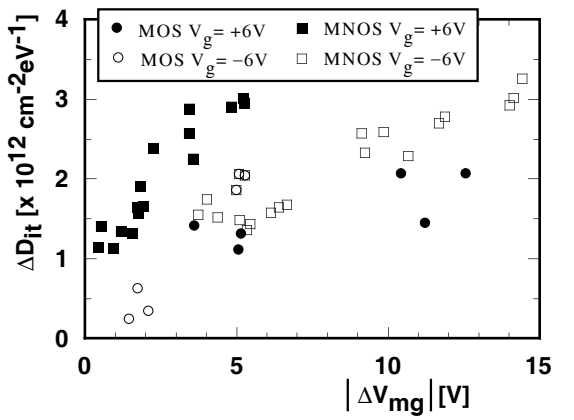

Figure 3: Radiation-induced D_{it} shift in MOS and MNOS structures as a function of the magnitude of V_{mg} shift.

4. Discussions

4.1 Charge trapping model

We discuss the charge trapping due to

irradiation by constructing a simple charge trap model as shown in fig. 4. In this model, we assumed that the hole traps are located in the oxide near Si-oxide (S-O) interface, and the hole and electron traps are located in the nitride near oxide-nitride (O-N) interface. N_{ho} and σ_{ho} are defined as the local density and the capture cross section of the hole traps in oxide, and N_{hn} and σ_{hn} (N_{en} and σ_{en}) are those of hole (or electron) traps in nitride. When the MNOS structure is irradiated, the electron-hole pairs are generated throughout the insulation layers, and a fraction that escaped initial recombination yields free electrons and holes. These free carriers are swept by electric field, and some of them are captured by the charge traps.

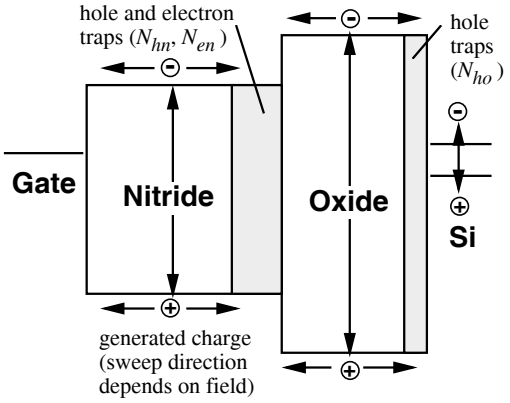

Figure 4: Charge generation and trapping model of MNOS structure under irradiation.

When the oxide and the nitride layers are irradiated by gamma rays of unit dose (ΔD), the electron-hole pairs ($\Delta\rho_{ox\,(ni)}$) are generated throughout the films as follows [6]:

$$\Delta\rho_{ox\,(ni)} = K_{ox\,(ni)} f_{yox\,(ni)}\, \Delta D\, d_{ox\,(ni)} \tag{1}$$

where $K_{ox\,(ni)}$ [C/cm^3/rad(SiO$_2$)] is the generation constant in the oxide (nitride) layer, f_y is the fractional charge yield that depends on the electric field. Benedetto *et al.* have evaluated these parameters as $K_{ox} = 1.30 \times 10^{-6}$ [C/cm^3/rad(SiO$_2$)] and $f_y = (0.27\ /(E_{ox} + 0.084) + 1)^{-1}$ in case of Co-60 gamma ray irradiation, where E_{ox} [V/cm] is the oxide field [7]. When V_g is positive, the generated holes in oxide drift toward the hole traps at S-O interface, and some of them are captured. The amount of captured hole (Δn_{ho}) can be expressed as:

$$\Delta n_{ho} = F_{ho}\, \sigma_{ho}\, [\, N_{ho} - n_{ho}\,] \quad , \tag{2}$$

where F_{ho} is the hole fluence at the traps, n_{ho} is the trapped hole density before irradiation of ΔD, and the capture cross section depends on the electric field as $E_{ox}^{-0.5}$ [8], [9]. When V_g is negative, the generated electrons drift toward the silicon. In this model, we assumed the charges are generated in silicon depletion layer by impact ionization due to injected electrons from oxide [10]. In that case, F_{ho} can be expressed as $\gamma \cdot \Delta\rho_{ox}$ where γ is the quantum yield. The amount of captured hole and electron by the traps at O-N interface may be calculated by the same manner as the S-O interface. The calculation of ΔV_{mg} is carried out by repeating the evaluation of radiation-induced trapped charge due to small amount of dose (ΔD = 2 krad(Si)) because the electric field in each insulator should be changed during irradiation.

In order to calculate ΔV_{mg}, the trapped charge density before irradiation have to be fed. We have ever reported the depth profile of fixed charge in the insulation layers [11], [12]. The profile was evaluated by slanted etching method, and it was found that the charges were located mainly at each interface, and the densities were obtained as:

$$Q_{so} = 1.6 \times 10^{-8}\ [\mathrm{C/cm^2}] \quad , \tag{3}$$

$$Q_{on} = 6.2 \times 10^{-8} - 5.2 \times 10^{-3}\, d_{ox}\ [\mathrm{C/cm^2}] \quad , \tag{4}$$

where Q_{so} and Q_{on} are the charge densities at S-O and O-N interfaces, respectively. Using these results, the charge density and the electric field before irradiation were defined.

4.2 Calculated results of ΔV_{mg}

The ΔV_{mg} of MOS structures are calculated by varying N_{ho}, σ_{ho} and γ. The lines in Fig. 1 show the fitted results, and it is found that the calcurated results can be fit to the experimental results by using following parameters: $N_{ho} = 5.0 \times 10^{18}$ cm^{-3}, $\sigma_{ho} = 2.0 \times 10^{-14}$ cm^2 (@ 1MV/cm), and $\gamma = 0.25$.

Next the ΔV_{mg} of MNOS structures are discussed. The charge trap density in the nitride layer and its profile have been investigated [13]-[15]. From these reports, we assumed that the electron and hole trap centers are distributed rectangularly within 10 nm from O-N interface in nitride layer as $N_{hn} = 1.2 \times 10^{20}$ cm^{-3} and $N_{en} = 2.0 \times 10^{19}$ cm^{-3}. In that case, the unknown parameters for calculation are σ_{hn}, σ_{en} and the charge generation coefficients in nitride (K_{ni} and f_{yni}). However K_{ni} and f_{yni} are very difficult to evaluate independently. So we assume the electric field dependence of f_{yni} is same as f_{yox}, and α is defined as:

$$\alpha = (K_{ni}\ f_{yni}) / (K_{ox}\ f_{yox}) \quad . \tag{5}$$

As the results of calculation, the calculated ΔV_{mg} can be fitted successfully to the experimental data by using following parameters: $\sigma_{hn} = 1.5 \times 10^{-16}$ cm^2 (@ 1MV/cm), $\sigma_{en} = 1.5 \times 10^{-14}$ cm^2 (@ 1MV/cm), and $\alpha = 2 \sim 5$ [%]. The lines in Fig. 2 show the fitted results.

From these fitting procedures, the small value of α was obtained. That indicates the amount of radiation-induced generated carriers in the nitride layer is much smaller than that in the oxide layer. In order to confirm the result physically, the photocurrents of MOS and MNS (Metal-Nitride-Si) structures are measured. The measurements were carried out using SEM system with 35 keV electron beam. The samples were set in a vacuum condition (1.5×10^{-6} Torr) to eliminate air ionization effects. Figure 5 shows the photocurrent densitiy as a function of the applied electric field during measurement. The insulator thickness of each sample is 100 nm. The current of MNS structure is about 10 ~ 20 % of the current of MOS structure under same electric field. From these results, it was confirmed that the charge generation rate due to irradiation in nitride is less than that in oxide. It is considered that the small generation rate in nitride is caused by the high initial recombination rate. However the detail discussions, for example the radiation source or the thickness dependence, are the subject for a future study.

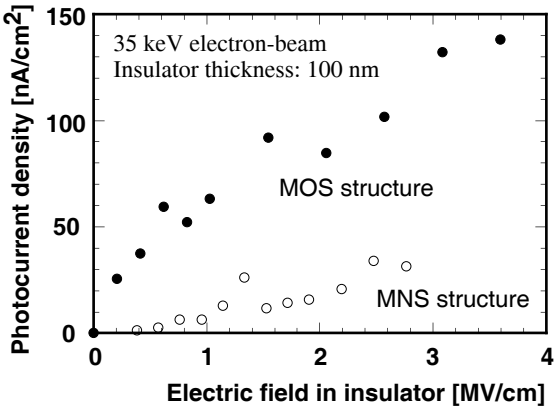

Figure 5: 35 keV electron-beam photocurrent densities of MOS and MNS structures as a function of electric field.

From above mentioned investigations, the charge trapping mechanism in MNOS structure under irradiation was clarified. When V_g is positive, the amount of radiation-induced trapped electrons at O-N interface is larger than that of holes at S-O interface because $N_{en} >> N_{ho}$, and is also larger

than that of holes at O-N interface because α is small. The effect of trapped electrons at O-N interface on ΔV_{mg} becomes large with nitride thickness, so the ΔV_{mg} changes from negative to positive with the thickness. And when the amount of electron increases, the oxide electric field is reduced. This reduction causes the decrease of the charge generation rate in oxide because the generated electron-hole pairs recombine easily under the weak field, and the amount of trapped electrons is saturated. When d_{ni} is thick, the oxide field can be suppressed by the small amount of trapped electrons because the initial field is weak, and the positive ΔV_{mg} is reduced. Therefore, ΔV_{mg} is saturated when nitride becomes thick. On the other hand when V_g is negative, the amount of trapped holes at O-N interface is larger than that of electrons. Hence the ΔV_{mg} is negative, and the shift increases with the increment of each insulator thickness.

From these results, it is confirmed that the proposed model is very useful to estimate the radiation-induced trapped charge in insulators of MNOS structure.

4.3 The optimum insulator thickness for radiation hardened structure

It is considered that the $\Delta V_{mg} = 0$ can be obtained using MNOS structure with specific oxide and nitride thicknesses when V_g is positive, as shown in Fig. 2. These thicknesses are considered to be the optimum thicknesses in terms of radiation-induced trapped charge. On the other hand, it was confirmed that the small ΔD_{it} is observed when ΔV_{mg} is small, as shown in Fig. 3. That indicates the insulation layer thicknesses of MNOS structure to minimize ΔV_{mg} is also optimum thicknesses for minimizing the radiation-induced interface state generation. In order to obtain these thicknesses, ΔV_{mg} of MNOS structures with varying d_{ox} and d_{ni} are calculated. Figure 6 shows the obtained optimum thicknesses with different radiation conditions when $V_g > 0$. In this figure, the equivalent oxide thickness is the same on each dashed line. It is found that the optimum thicknesses do not depend much on the total dose and on the gate voltage during irradiation when the equivalent oxide thickness is less than about 100 nm. It was also confirmed that ΔV_{mg} of MNOS structure is almost same as that of MOS structure which has same equivalent oxide thickness when $V_g < 0$. From these results, it is expected that the radiation hardened device can be achieved using MNOS structure in terms of total dose effects.

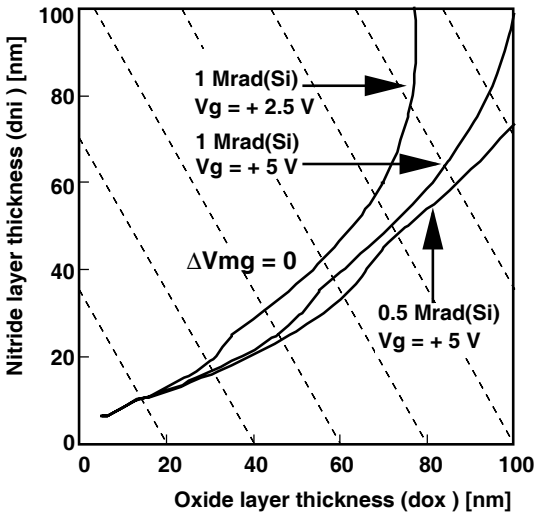

Figure 6: The optimum insulator thicknesses of MNOS structures with different radiation conditions when $V_g > 0$. The equivalent oxide thickness is the same on each dashed line.

5. Conclusions

The charge trapping in the insulation layers in MNOS structure under irradiaiton has been investigated by analyzing ΔV_{mg}. The direction and the magnitude of ΔV_{mg} depended on the insulation

layer thickness and the applied gate voltage during irradiation. ΔV_{mg} was calculated by a proposed simple charge trap model. The calculated results could be fitted to the experimental results by varying the densities and the capture cross sections of the charge trap centers, and these parameters were obtained. It is considered that these parameters may be changed by the fabrication processes. We considered the studies on the process dependencies of these parameters are helpful to verify the generality of our model. From these results, the charge trapping mechanism under irradiation was clarified.

The strong correlation was observed between ΔV_{mg} and ΔD_{it}. That indicates the insulator thicknesses to minimize ΔV_{mg} are the optimum thicknesses for radiation hardened device in terms of not only radiation-induced trapped charge but also interface state generation. The thicknesses were evaluated by the model calculations when V_g is positive. It was found that the optimum thicknesses do not depend much on the total dose and on V_g when the equivalent oxide thickness is less than about 100 nm.

From these results, it was found that the charge trap model is very useful to understand the charge trapping mechanism in the insulators of MNOS structure under irradiation, and the MNOS structure can be applied to the radiation hardened device.

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References

[1] K. H. Zaininger and A. G. Holmes-Siedle, R. C. A. Review. 28, 208 (1967).
[2] K. Watanabe, M. Kato, T. Okabe, and M. Nagata, IEEE Trans. Nucl. Sci. NS-33, 1216 (1986).
[3] C. W. Perkins, K. G. Aubuchon, and H. C. Dill, IEEE Trans. Nucl. Sci. NS-15, 176 (1968).
[4] P. F. Schmidt, M. J. Rand, J. P. Mitchell, and J. D. Ashner, IEEE Trans. Nucl. Sci. NS-16, 211 (1969).
[5] J. R. Cricchi and D. F. Barbe, Appl. Phys. Lett. 19, 49 (1971).
[6] H.E. Boesch, Jr., F.B. McLean, J.M. Benedetto, and J.M. McGarrity, IEEE Trans. Nucl. Sci. NS-33, 1191 (1986).
[7] J.M. Benedetto and H.E. Boesch, Jr., IEEE Trans. Nucl. Sci. NS-33, 1318 (1986).
[8] C.M. Dozier and D.B. Brown, IEEE Trans. Nucl. Sci. NS-27, 1694 (1980).
[9] H.E. Boesch, Jr., and F.B. McLean, IEEE Trans. Nucl. Sci. NS-32, 3940 (1985).
[10] C. Chang, C. Hu, and R.W. Brodersen, J. Appl. Phys. 57, 302 (1985).
[11] Y. Takahashi and K. Ohnishi, Electronics and Communications in Japan, Part 2, 82, 10 (1999).
[12] Y. Takahashi, K. Ohnishi, T. Fujimaki, and M. Yoshikawa, IEEE Trans. Nucl. Sci. NS-46, 1578 (1999).
[13] Y. Kamigaki, S. Minami, and H. Kato, J. Appl. Phys. 68, 2211 (1990).
[14] F. Martin and X. Aymerich, Thin Solid Films. 221, 147 (1992).
[15] Y.C. Park, W.B. Jackson, N.M. Johnson, and S.B. Hagstrom, J. Appl. Phys. 68, 5212 (1990).

研究課題名：光励起プロセスによるシリコン系絶縁膜の低温成長

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【研究目的】

近年の半導体集積回路の微細化に伴い，シリコン酸化膜の薄膜化は限界に近づいており，比誘電率が酸化膜より大きな，シリコン窒化膜のゲート絶縁膜への応用について注目されている．一方，p^+ポリシリコンゲートを有する MOSFET において, ポリシリコン作製時のゲート酸化膜でのボロンつき抜け現象による基板不純物濃度変化に起因したしきい値電圧変動は，デバイスの信頼性確保の上で大きな問題となっている．窒化膜および窒化酸化膜は，酸化膜に比べボロンつき抜け現象を抑制できる絶縁膜として報告されているが，その作製過程では高温熱処理などを必要とするものが多い．更なる集積度向上，基板の大口径化を考慮すると，プロセス温度の低温化が必要である．そこで，光励起反応を用いたシリコン窒化膜の低温成長の確立を目的に検討を行った．

一方，電子デバイス等の作製において不可欠な絶縁膜であるシリコン酸化膜の製膜においても，同様に低温化が要求されている．本研究では純水を用いた陽極酸化法に着目し，陽極酸化膜の特性評価および酸化メカニズムの解明を目的に，光照射を含めたプロセス条件に対する各種膜特性について検討を行った．

【研究概要】

これまでに，アンモニアおよびジクロルシランを材料ガスとした光 CVD 法について検討を行ってきた．その結果，波長 254，185nm にピークを有する紫外光を用いることにより基板温度 300℃程度で比較的良質なシリコン窒化膜が堆積可能であることを示した．本研究では，紫外線照射アンモニアガスによるシリコン基板の直接窒化について検討を行った．減圧アンモニアガス雰囲気中（300Pa）のシリコン基板に紫外光（波長 : 254，185nm）を照射した試料表面を組成分析した結果，基板温度 200℃以下の低温で直接窒化が進行可能であることを確認した．また，エリプソメータを用いて膜厚および屈折率の測定を行った結果, 窒化時間を増加させても膜厚は約 2nm 程度で飽和する傾向があること，作製膜の屈折率は 2.2ー2.3 程度であることがわかった．また，本手法により作製した窒化膜を用いてアルミゲート MIS 構造を作製し，電気的測定を行ったところ，MIS 構造特有の容量−電圧特性が得られることがわかったものの, 低電界時におけるリーク電流が LPCVD 法などにより作製した窒化膜に比べて非常に大きくなることを確認した．一方，窒化後の基板を乾燥酸化法により酸化することにより，窒素が数%程度混入した窒化酸化膜の作製が可能であることを確認し，その酸化速度は窒化処理を施さない基板に比べて非常に遅くなることがわかった．

一方，これまでに純水を用いた陽極酸化法により，シリコン上に室温にて酸化が進行することを示した．本研究では，酸化後の熱処理温度に対する膜特性変化について評価した．その結果，熱処前の酸化膜では低電界印加時に大きなリーク電流が観測されたものの，800℃以上の熱処理により熱酸化膜同等の良好な絶縁特性を示すことが明らかとなった．また，赤外吸収分析（FT-IR）を行った結果，熱処理温度の上昇に伴い，水素脱離により Si-OH 結合のピークが低下することを確認した．また，基板表面のキャリア密度が成長速度に与える影響を評価するため，自由電子レーザを照射しながら陽極酸化を行った．その結果，光照射による製膜中の回路電流および成長速度の増大を

確認した．

【まとめ】

紫外線のエネルギーを用いることにより，アンモニアガスを用いてシリコンを200℃以下の低温で直接窒化できることを明らかにした．また，その成長速度は非常に低く，極薄膜の膜厚コントロールが可能であることがわかった．今後，自由電子レーザを用いた波長の最適化などにより，膜質の改善を行って行きたいと考える．

また，純水を用いた陽極酸化膜に対し，製膜後熱処理を施すことにより絶縁特性が改善することを明らかにした．これは，熱処理による水素脱離によるものと考えられる．また，製膜中の光照射について検討を行った結果，光照射により成長速度が増大することを確認した．今後これらの原因について詳細に検討を行って行きたいと考える．

【研究業績等】

・発表論文

(1) K. Ohnishi, A. ito, Y. Takahashi and S. Miyazaki: “Growth and Characterization of Anodic Oxidized Films in Pure Water”, Jpn. J. Appl. Phys., Vol.41, No.3A, pp.1235-1240, 2002.3.

・学会発表

(1) K. Ohnishi and A. Ito (2000) Characterization of Anodic Oxide Films in Pure Water, Proc. of the 3rd International Symposium on Advanced Science and Technology of Silicon Materials
(2) 伊藤鑑，大西一功，高橋芳浩 (2000) 純水中での陽極酸化法により作製した SiO2 膜に関する研究，応用物理学会関係連合講演会
(3) 川倉秀雄，高橋芳浩，大西一功 (2000) 光 CVD 法により作製したシリコン窒化膜の熱処理効果，応用物理学会関係連合講演会
(4) 宮崎俊助，大西一功，高橋芳浩 (2001) 陽極酸化法により作製した酸化膜の熱処理効果，応用物理学会関係連合講演会
(5) 森田崇，臼倉一敏，大西一功，高橋芳浩 (2002) 紫外線励起アンモニアガスを用いた酸窒化膜の作製・評価，応用物理学会関係連合講演会
(6) 渡辺竜太，柴田徹也，新垣久，藤田明良，高橋芳浩，大西一功 (2004) 陽極酸化法で作製したシリコン酸化膜の特性，応用物理学関係連合講演会
(7) 柴田徹也，渡辺竜太，新垣久，藤田明良，高橋芳浩，大西一功 (2004) 陽極酸化法によるシリコン酸化膜の作製と評価，応用物理学関係連合講演会

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Growth and Characterization of Anodic Oxidized Films in Pure Water

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An anodic oxidized film has been deposited in pure water at room temperature. Film thickness increases linearly as a function of total charge during oxidation. High film deposition rate and low surface roughness are obtained by alternately changing the polarity of the applied voltage. The film growth mechanism is discussed and the model of anodic oxidation in pure water is proposed. The HF etching rate and the oxide thickness are reduced by an increase in annealing temperature. Though the electrical characteristics of the anodic oxide film are inferior to those of the film obtained by thermal oxidation, they can be improved by thermal annealing at a temperature of 400°C. [DOI: 10.1143/JJAP.41.1235]

KEYWORDS: silicon dioxide, anodic oxidation, low-temperature process, thermal annealing

1. Introduction

With the progressive shrinking of LSI device size, device and circuit is complexity increasing. The fabrication process is also becoming increasingly difficult. Moreover, there is a great demand to reduce energy consumption on the grounds of preventing global warming and environmental pollution. An oxidation process in VLSI fabrication requires a high temperature of around 1000°C and thermal stress damages the silicon wafer inconspicuously. From this viewpoint, low-temperature processes have been researched. Many low-temperature processes have been proposed to fabricate insulation films on silicon such as plasma deposition, chemical vapor deposition (CVD), photo-CVD,[1] jet vapor deposition (JVD),[2] anodic oxidation and so on.

We considered the possibility of applying the electrical effect to the fabrication process of semiconductor devices at low temperatures. The first thing we noted was the occurrence of electrically enhanced oxidation and anodic oxidation on the Si substrate. The effect of the electric field on oxidation has been studied previously.[3] Anodic oxidation has been experimentally studied previously as an oxide formation process. Usually, anodic oxidation was carried out with electrolytes such as N methylacetamide (NMA)–KNO_3 or tetrahydrofurfutyl alcohol (THF)–KNO_3.[4–6] An anodic oxidized silicon film in pure water was also reported by Dubrovskii *et al.*[7]

Early works on anodic oxidation reported that the etching rate was greater than that of thermal oxides and was changed by impurity solutions and the growth rate was a function of applied voltage in constant current mode.[5,6] There is a controversy regarding the oxidation mechanism. Dubrovskii *et al.* proposed the silicon diffusion model in which silicon ions diffused to the oxide–electrode boundary and formed the oxide,[7] whereas Kraitchman and Oroshnik argued that the oxygen migrates close to the oxide–silicon interface and oxide growth occurs at the interface.[5]

Although the electrical property is improved by high-temperature annealing in He, the oxide films were substantially porous and the electrical property was poor. For these reasons, the use of anodic oxidation was abandoned in integrated circuit fabrication processes.

We intend to study the application of the electrical effect in the fabrication of integrated circuits at low temperatures. This will contribute to suppressing the energy consumption in VLSI fabrication systems. Here, we report on the experimental method and the characteristics of anodic oxidized silicon dioxide films grown in pure water at room temperature as a possible oxidation process at a low temperature. We discuss the electric characteristics and growth mechanism. We clarify that the surface roughness of the oxide is improved by alternately changing the polarity of the applied voltage and that the oxide thickness is not increased by the applied voltage, but increases with the total charge flowing between electrodes during oxidation. The electrical characteristic is improved by annealing over 400°C after oxidation.

2. Experimental

Samples used in our experiments were fabricated as shown in Fig. 1. Wafers used in this experiments were n-type and p-type silicon wafers of ⟨100⟩ plane and their corresponding resistivities were 3–5 Ω·cm and 0.8–1.2 Ω·cm. The wafers were cleaned by ths standard RCA cleaning method. Anodic oxidation was carried out in pure water with resistivity of 16 MΩ·cm at 20°C. After oxidation, wafers were annealed in nitrogen atmosphere at various appropriate temperatures. A reference sample was prepared by thermal oxidation at 1045°C in dry oxygen and annealed at the same temperature in nitrogen. Film thickness was

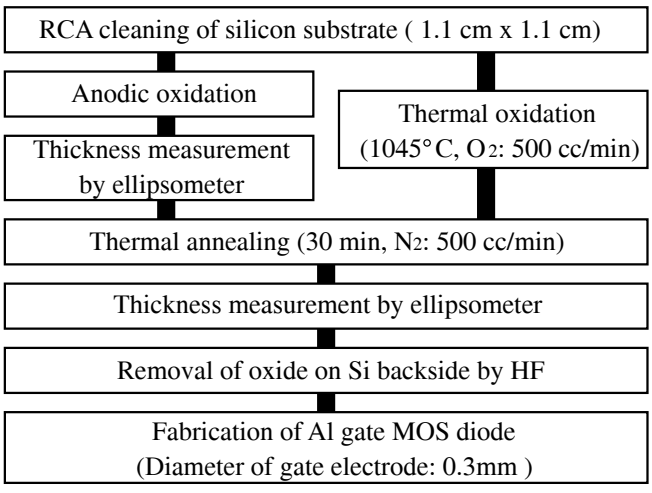

Fig. 1. Sample preparation process flow.

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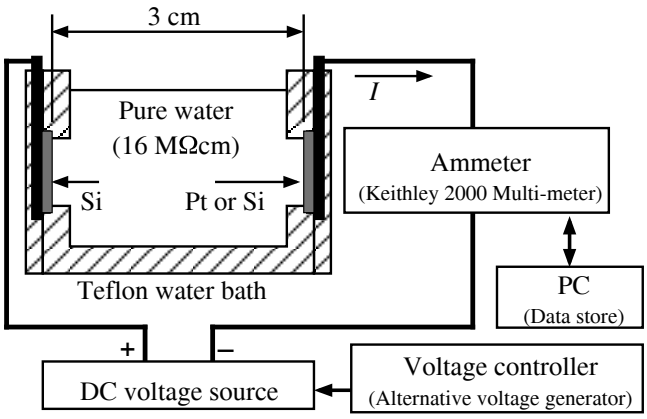

Fig. 2. Anodic oxidation experimental system.

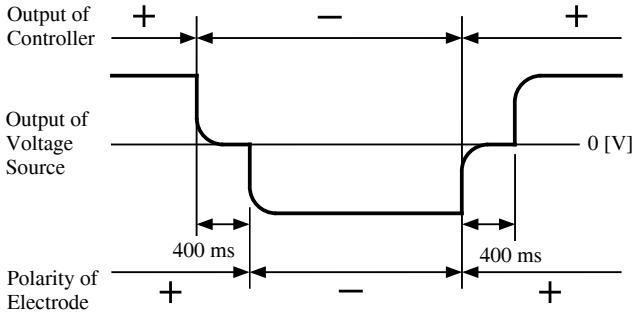

Fig. 3. Time chart of alternately changed polarity of voltage (AC).

measured by the ellipsometry method. The film composition was analyzed by X-ray photoelectron spectroscopy. Electrical properties were measured using MOS structures with aluminum electrodes. Anodic oxidation was carried out in pure water with the application of a constant voltage across the silicon wafer anode and the other electrode of platinum or silicon, as shown in Fig. 2. The distance between the electrodes was 3 cm, and anodic oxidation was carried out with a constant DC voltage or by alternately changing the polarity of the voltage (AC). We used the period of 60 s and the duty ratio of 0.5 for the AC voltage source. Figure 3 is a time chart of applied voltage when the polarity changes alternately. The current flow during anodic oxidation was monitored and integrated to calculate the total charge during oxidation. Silicon substrates were cut to a 1.1 cm square size, and the anodic oxidation window was 1 cm square.

3. Experimental Results

We measured distributions of the thickness of both samples fabricated with DC and AC voltages. Figure 4 shows profiles of oxide films in this experiment. Figures 4(a)

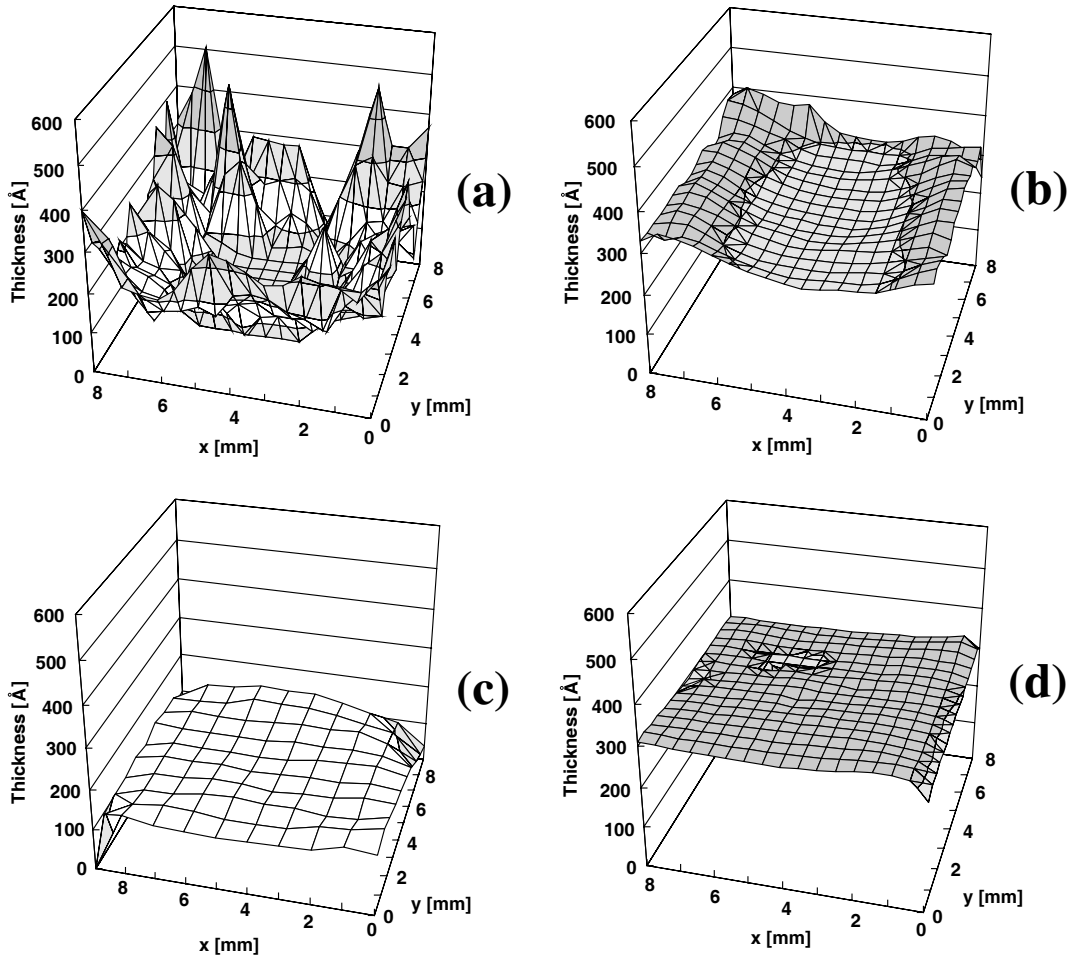

Fig. 4. Profile of oxide thickness. (a) on n-Si with 300 V DC (b) on p-Si with 300 V DC (c) on n-Si with 300 V AC (d) on p-Si with 300 V AC.

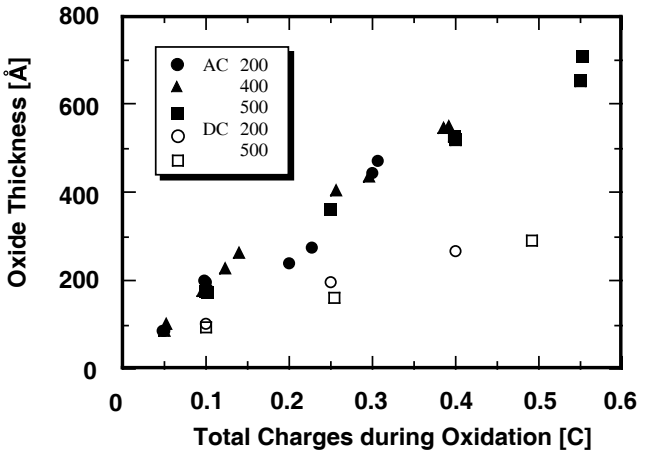

Fig. 5. Film thickness vs total charges during anodic oxidation on p-type (100) 3–5 Ω·cm Si at 20°C.

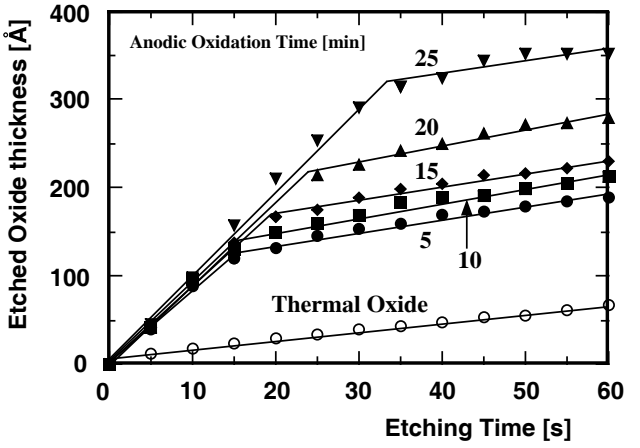

Fig. 6. Etched oxide thickness vs etching time for different anodic oxidation times.

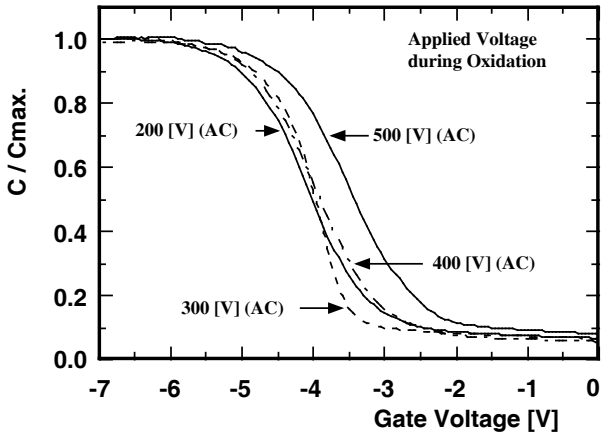

Fig. 7. *C–V* curves of MOS structures with anodic oxide fabricated at different voltages.

and 4(b) show thickness distributions of the oxide film on the n-type and p-type silicon substrates when the voltage was 300 V DC. Figures 4(c) and 4(d) show distributions of the oxide thickness when the applied voltage changed polarity as shown in Fig. 3. The oxide on the n-type substrate was thinner than that on the p-type substrate and randomly distributed, but it was improved upon oxidation with an applied AC voltage as shown in Fig. 4(c). Figure 5 shows the oxide thickness on the p-type silicon substrate against the total charge flowing in the system during oxidation for different applied voltages. This figure shows that the oxide film thickness linearly increased with total charges during oxidation and the oxide obtained with AC voltage is thicker than that obtained with DC voltage. The oxide thickness as a function of total charges flowing during oxidation with AC voltage is twice that with DC voltage. The composition of the anodic oxidized film in our experiment was analyzed by X-ray photoelectron spectroscopy; it was stoichiometric SiO_2, the same as the thermal oxide formed at 1045°C.

We estimated the etching rate of thermal oxide and anodic oxide films in order to compare the quality. The thermal oxide film of 30 nm thickness was grown on a p-type silicon substrate at a temperature of 1045°C and then it was reoxidized by anodic oxidation with 300 V AC for 5–25 min. These samples were etched by a solution of HF(48%) : $H_2O = 1 : 50$ at room temperature. Figure 6 shows the etched oxide thickness against etching time for various anodic oxidation times. The region of high-etching rate at an early stage is predominantly of anodic oxide and the region of low-etching rate a later stage is predominantly thermal oxide being slightly affected by anodic oxidation. This result reveals that the density of anodic oxide is lower than that of thermal oxide as reported previously. The etching rate of the thermal oxide film is 1 Å/s, and 8–9 Å/s for the reoxidized film by anodic oxidation. It is confirmed that the etching rate of the oxide film fabricated by anodic oxidation (300 V AC) on the silicon substrate is 25 Å/s, and the rate of the film grown with DC voltage is higher than that with AC voltage.

The refractive index of the anodic oxide film was around 1.45 for films thicker than 200 Å, however it ranged from 1.3 to 1.4 for films thinner than 100 Å. The dielectric constants were determined using the thickness measured by ellipsometry and the capacitance measured under accumulation condition. The estimated dielectric constant was between 4 and 7 and it was higher than that of the thermal oxide.

The electrical characteristics are analyzed from high-frequency *C–V* and *I–V* characteristics. Figure 7 shows the *C–V* curves for different anodic voltages and Fig. 8 shows the density of Si/SiO_2 interface states evaluated by the Terman method. Densities of fixed positive charge in the oxide are evaluated by flat-band voltages, and $4.5–4.7 \times 10^{12}\ cm^{-2}$ and $3.2 \times 10^{12}\ cm^{-2}$ are obtained when the applied voltages during oxidation are 200–400 V and 500 V (AC), respectively.

Anodic oxidized films were annealed in nitrogen atmosphere at various temperatures. The etching rate and also thickness decrease as the temperature increases as shown in Figs. 9 and 10.

Electrical characteristics are improved by high-temperature annealing. Figure 11 shows the *C–V* curve of a MOS structure annealed in nitrogen atmosphere at 400°C for 30 min. The anodic oxidized film is fabricated with 300 V AC and the total charge during oxidation is 0.1 C. The density of fixed positive charge is $4.3 \times 10^{11}\ cm^{-2}$. Figure 12 shows the density of $Si–SiO_2$ interface states of the same

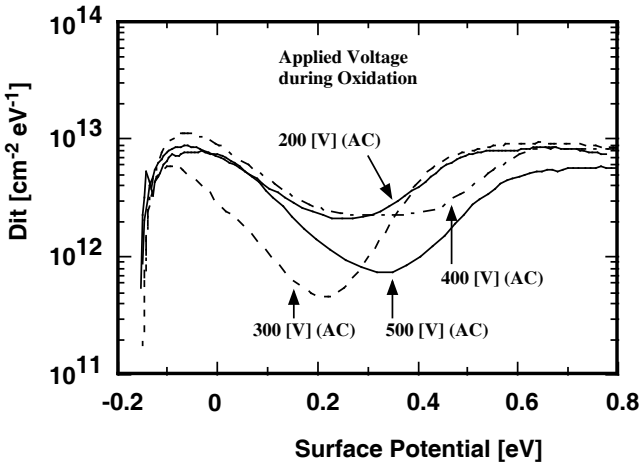

Fig. 8. Interface states density vs surface potential evaluated from *C–V* curves in Fig. 7.

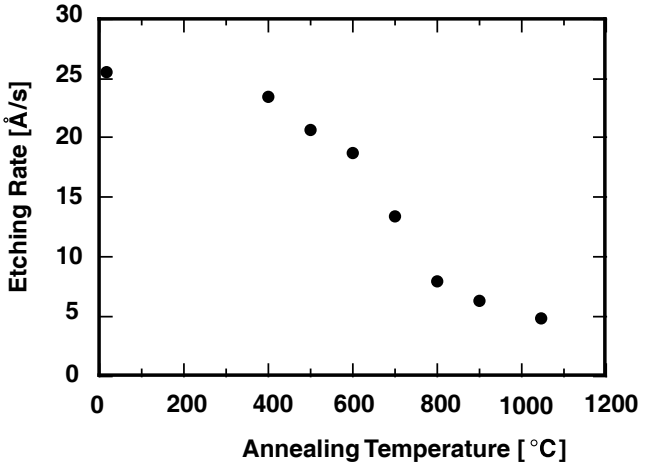

Fig. 9. Etching rate of anodic oxide after annealing in N_2 atmosphere for 30 min at different temperature. Anodic oxidized with DC voltage and total charge is 1 C.

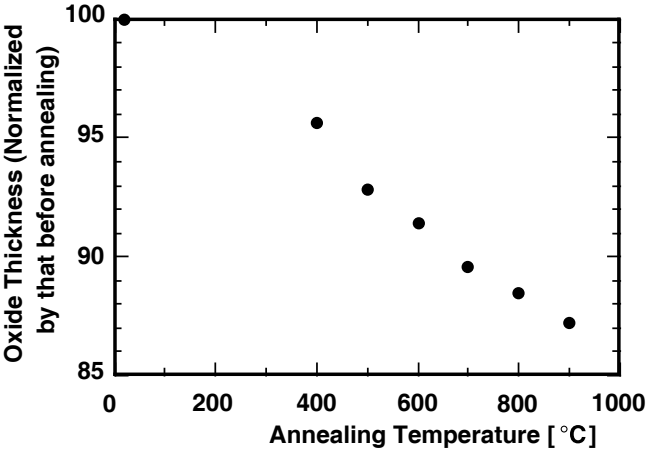

Fig. 10. Thickness change at different annealing temperature in nitrogen atmosphere for 30 min. Anodic oxidation condition is the same as in Fig. 9.

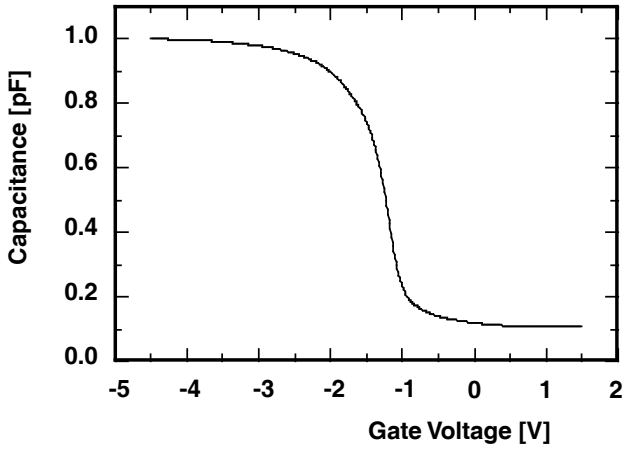

Fig. 11. *C–V* characteristic of a MOS structure after annealing at 400°C for 30 min. Anodic oxide is fabricated at 300 V AC, total charge is 0.1 C.

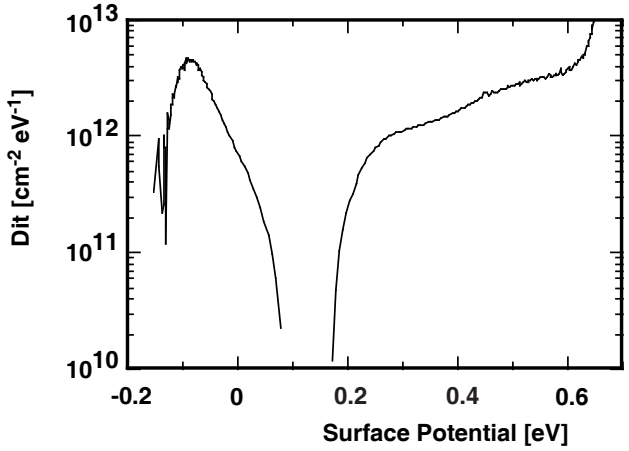

Fig. 12. Interface states density vs surface potential evaluated from *C–V* characteristic of Fig. 11.

structure.

4. Discussions

In this paper, we explain our experimental results of anodic oxidation on the silicon substrate in pure water at room temperature. The growth rate of the oxide film on the n-type substrate is smaller than that of the oxide film on the p-type substrate and SiO_2 grows only under the condition that the voltage of the silicon wafer is positive. The thickness of the oxide film increases as the total charge during oxidation progresses; this result differs from that of Dubrovskii's experiment. Oxidation by alternately changing the voltage polarity makes the surface roughness decrease. The oxidation rate on the p-type substrate is larger than that on the n-type substrate and moreover, the surface flatness of the anodic oxide film on the n-type substrate is poorer than that on the p-type substrate. When the electrode polarity changes alternately, the oxide growth rate is twice that of the case of single polarity and the surface roughness of the oxide film on the n-type substrate is improved.

From these experimental results, we will consider the anodic oxidation mechanism as follows. A water molecule has a small dipole moment. Electrons of hydrogen atoms take positions close to the oxygen atom side. A hydrogen

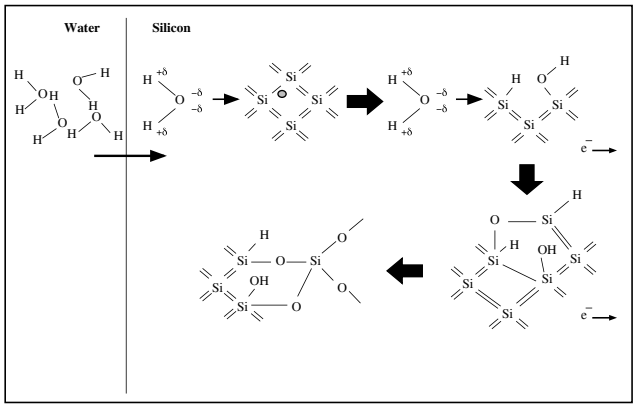

Fig. 13. Proposed model of anodic oxidation in pure water.

atom is slightly positively charged, $+\delta$, and the oxygen of a water molecule is slightly negatively charged, -2δ as shown in Fig. 13. When the silicon wafer is biased positive against a cathode, positive charges exist at the water–Si interface. Oxygen of a water molecule is directed toward the positively charged Si–water interface as shown in Fig. 13.[8] The water molecule drifts and/or diffuses into the silicon bulk, and hydrogen is dissociated from H_2O. This hydrogen is highly activated and reacts with Si=Si bonds and/or dangling bonds forming SiH and also breaks the covalent bond of Si=Si. The oxygen-hydrogen pair atom combines with Si and forms SiOH.

When a negative bias is applied to the silicon substrate, the hydrogen of a water molecule is directed toward the Si-water interface and the water molecule is dissociated to hydrogen and hydroxyl by reacting with electrons from the negative electrode.[5] Hydrogen drifts and/or diffuses into the silicon bulk and reacts with Si=Si forming Si–H. OH drifts out to the water. Another possible mechanism is that OH and H in the water are dissociated from a water molecule and H drifts and/or diffuses into the silicon bulk and forms Si–H and/or is positioned at an interstitial site. The hydrogen diffuses deeply into the inner space of the silicon bulk due to a large diffusion constant.

When the polarity of the supplied voltage to the silicon substrate is changed from negative to positive, electrons move from the Si–metal interface to the water–Silicon interface and the distributed ions at the interface are neutralized by the electrons. Moreover, activated hydrogen remaining in the oxide approaches the water–Si interface. The hydrogen distributed in the silicon bulk breaks the Si=Si bond and forms Si–H, and OH from the water–Si interface forms the Si–O and SiO_2 as shown in Fig. 14. Thus the oxidation rate against total charges during oxidation in case of AC voltage is roughly twice that with DC voltage as shown in Fig. 5. In the case of the p-substrate, holes accumulate sharply at the interface as shown in Fig. 15. Meanwhile, in the case of the n-substrate, donor ions form a depletion layer, holes (minority carrier) are present at the interface as shown in Fig. 16 and a depletion layer restricts the growth rate.

The growth rate difference between SiO_2 on the n-type substrate and on the p-type substrate is considered as follows. In case of the p-type silicon substrate, positive

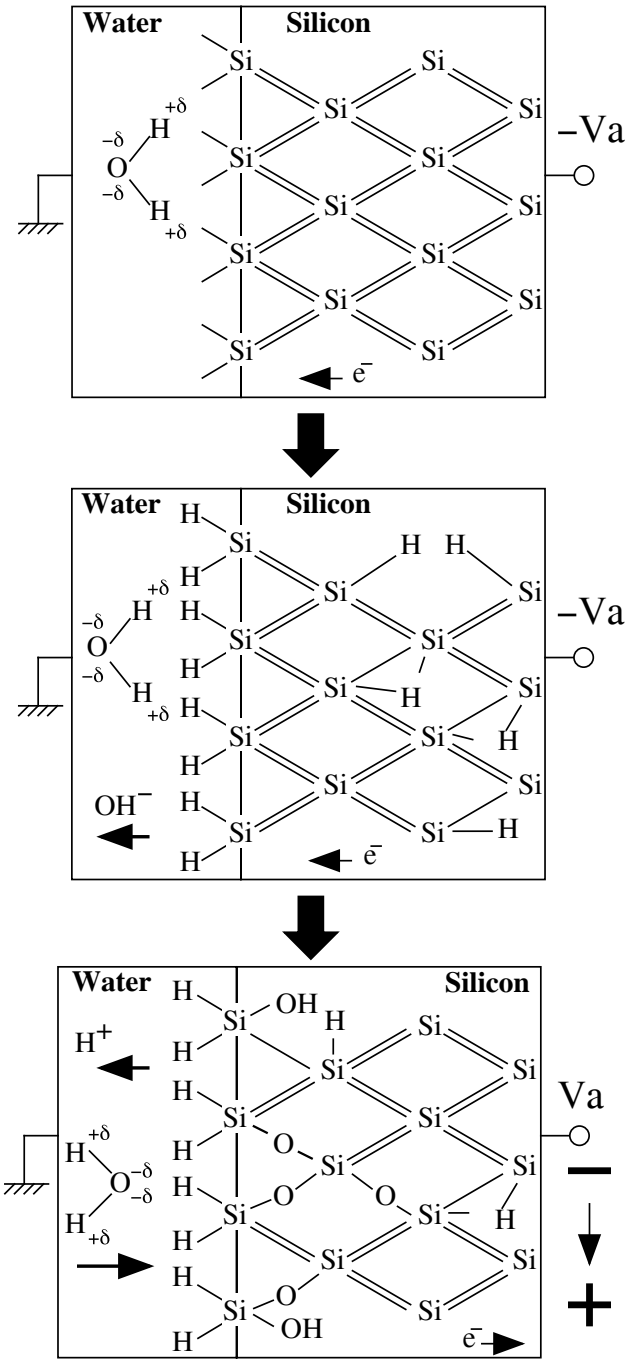

Fig. 14. Anodic oxidation model when the applied voltage changes from negative to positive.

charges near the water–Si interface are holes and are sharply distributed at the silicon surface. Therefore, OH and H react easily with silicon covalent bonds and dangling bonds, and form SiOH and SiH, respectively. In the case of an n-type silicon substrate, positive charges near the water–Si interface are ionized donors and holes that are minority carriers in an n-type substrate. There is a small number of holes compared with the case of the p-type substrate. Thus, the number of H and OH reacting with holes is smaller than for the p-type substrate.

5. Conclusions

We experimented with anodic oxidation in pure water at

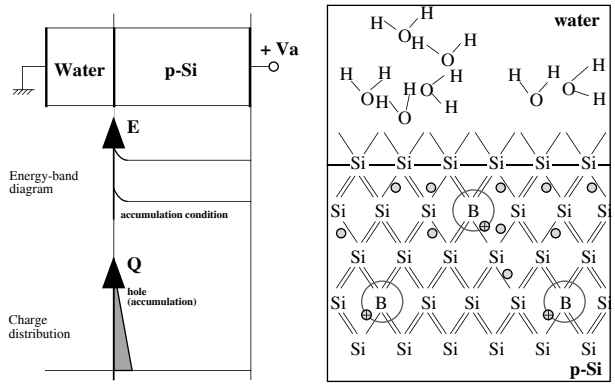

Fig. 15. Energy band diagram and charge distribution of n-Si surface.

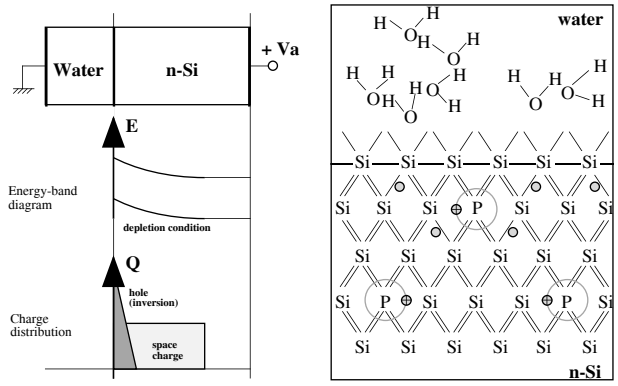

Fig. 16. Energy band diagram and charge distribution of p-Si surface.

room temperature as a possible low-temperature process and also discussed the growth mechanism using a model of molecular dipoles of water. We found that alternately changing the polarity of the applied voltage operates effectively to cause anodic oxidation. We also found that the composition of the oxide was stoichiometric SiO_2, the oxide thickness increased with charges flowing during oxidation and the growth rate on p-type silicon was higher than on n-type silicon. The surface roughness was larger on n-type silicon than on p-type silicon. When the applied voltage polarity was changed alternately, surface roughness became small and the growth rate became twice that in the case of single polarity.

We also examined the possibility of improving the electrical characteristic of SiO_2 films by high-temperature annealing. The etching rate of the oxide film became small, and it was effective in decreasing the density of Si/SiO_2 interface states and positive charge density in the oxide.

Our intention in performing this study is to apply the anodic oxide for the following purposes.

1. Low-temperature VLSI processes.
2. Bonded and Etched SOI.
3. Oxide film for micro-machining.

It is difficult to apply the anodic film to the LSI insulating film process directly. However, it will be possible to improve the quality by controlling the resistivity of pure water, substrate temperature and voltage stability. If the anodic oxide can be applied to an oxidized substrate to fabricate a BE–SOI wafer, an inexpensive SOI substrate can be obtained. We consider that the most realistic application at this stage is the use of the anodic oxide for micro-machining.

We attempted to apply the anodic oxidation to aid the suppression of global warming and environmental pollution, and made a tiny step toward the application of the electrical effect to the device fabrication process. We hope this study will contribute to positive changes in the use of energy.

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1) Y. Numasawa, K. Yamasaki and K. Hamano: Jpn. J. Appl. Phys. **22** (1983) 792.
2) X. Wang, T. P. Ma, G. Cui, T. Tamagawa, J. W. Goltz, S. Karechi, B. H. Halpern and J. J. Schmitt: Jpn. J. Appl. Phys. **34** (1995) 955.
3) P. J. Jorgensen: J. Chem. Phys. **37** (1962) 874.
4) E. F. Duffek, C. Myroie and E. A. Bejamini: J. Electrochem. Soc. **111** (1964) 1042.
5) J. Kraitchiman and J. Oroshnik: J. Electrochm. Soc. **114** (1967) 405.
6) A. G. Revesz: J. Electrochem. Soc. **114** (1967) 629.
7) L. A. Dubrovskii, V. G. Mel'nik and L. L. Odynets: Russ. J. Phys. Chem. **36** (1962) 1183.
8) J. P. Hogan, A. M. Stoneham and M. Jaros: Philos. Mag. B **55** (1987) 225.